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EXAMINER	
CARTER III, ROBERT E	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,672	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	ROBERT E. CARTER III	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 02/12/2008 has been entered and considered by the examiner.

Information Disclosure Statement

2. The IDS submitted on 02/11/2008 listed the incorrect application number. The number listed was 10/521678, while the correct application number for the instant application is 10/521672. The rest of the information given on the IDS was correct for the instant application, and therefore the examiner has corrected the application number on the submitted IDS and has entered and considered the IDS as part of the case. Because the examiner has made these corrections, the applicant is not required to re-submit the IDS submitted on 02/11/2008.

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Please include the following references from the specification in an IDS statement to make the record clear:

The references listed below should be provided so that they can be considered.

UA-A-5130829

Please include copies of any of the above references per 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al. (US Patent # 6,256,076) in view of Greene et al. (US Patent # 6,667,783).

As for claim 1, Bae et al. (Fig. 24) discloses:

An active matrix liquid crystal display device comprising:

an array of pictures elements (Fig. 24), *each including a picture element electrode* (CLC) *and a switching device* (Q), *located at respective intersections between crossing sets of selection* (GL) *and data* (DL) *address conductors connected to the picture elements; wherein each picture element includes a storage capacitor* (CST) *connected between the picture element electrode and a capacitor line* (line of storage capacitors CST connected in a row) *shared by the picture elements in the same row, and wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements* (the left end of the capacitor lines are connected to the previous gate lines).

Bae et al. does not teach a set of connection lines supplying signals to the selection address conductors.

In the same field of endeavor (i.e. LCD structures) Greene et al. (Fig. 9c) discloses:

a set of connection lines (200) *for supplying selection signals to the set of selection*

address conductors (186), *which connection lines extend from one side of the array* (Access Side) *in the direction of the set of data address conductors* (182) *and are connected* (210) *to respective ones of the set of selection address conductors,*

combining Bae et al. and Greene et al. would meet the claimed limitations:

wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements so that each connection line is connected to a respective selection address conductor for one row of picture elements and its coupled capacitor line for another row of picture elements.

Since Bae et al. teaches selection address conductors coupled to capacitor lines and Greene et al. teaches connection lines connected to selection address conductors the obvious combination of the references teaches connection lines connected to selection address conductors and capacitor lines.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Bae et al. by adding the connecting lines of Greene et al. to improve sharpness, contrast, and display form factor (Greene et al., Col. 7, lines 12-18).

As for claim 2, Bae et al. teaches:

wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with an adjacent row of picture elements (the left end of the capacitor lines are connected to the previous gate lines).

As for claim 3, Bae et al. teaches:

wherein a selection address conductor and a capacitor line are coupled by an interconnection between their ends at one side of the array (the left end of the capacitor lines are connected to the previous gate lines).

As for claim 4, Bae et al. as modified by Greene et al. teaches the limitations of claim 1.

Bae et al. as modified by Greene et al. does not teach:

wherein the interconnections for successive selection address conductors and their respective associated capacitor lines are arranged alternately at opposite sides of the array.

However, the display device defined by the limitations of claim 4 is electrically equivalent to the display device of Bae et al. as modified by Greene et al. as used in the rejection of claim 1 above. Therefore the limitations of claim 4 are simply that of design choice, and at the time of the invention making such design choices would have been obvious to one of ordinary skill in the art to do so as to optimize circuit layout for manufacturing of the display device.

Yasui (US Patent # 4,822, 142) discloses an exemplary LCD display with interconnections of selection address conductors arranged alternately at opposite sides of the array (the conductors are connected to the next conductor inside the drivers 17 and 17')

As for claim 5, Greene et al. teaches:

wherein each connection line (200) *extends from one side of the array* (Access Side) *and is connected at a connection point* (210) *to the selection address conductor* (186)

with which it is associated that is closest to that side, and wherein the connection line terminates at that connection point.

As for claim 7, Bae et al. teaches:

wherein the picture element array is driven using a capacitively coupled drive scheme in which part of the drive voltage applied to the picture element electrode is provided via the storage capacitor (Fig. 12, Col. 9, lines 24-33, The storage capacitor is charged when driving and maintains the drive voltage on the pixel).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al. in view of Greene et al. as applied to claims 1-5, and 7 above, and further in view of Fujikawa et al. (US Patent # 5,995,177).

As for claim 6, Bae et al. as modified by Greene et al. teaches the limitations of claim 1.

Bae et al. as modified by Greene et al. does not teach the capacitor line and selection address conductor of a row of picture elements extending along opposite sides of the row.

In the same field of endeavor (i.e. LCD displays with capacitor lines) Fujikawa et al. discloses:

wherein the capacitor line (3) and selection address conductor (2) associated with one row of picture elements extend along opposite sides of the row of picture elements

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the selection address conductors and capacitor

lines of Bae et al. as modified by Greene et al. with the layout of the ones in Fujikawa et al. to reduce manufacturing steps while maintaining satisfactory contact points (Fujikawa et al., Col. 5, lines 23-30).

Response to Arguments

9. Applicant's arguments filed 02/12/2008 have been fully considered but they are not persuasive.

Regarding the title, applicant argues:

"the Examiner has requested that a new title be submitted, asserting that the title of the invention is not descriptive.

The Applicant respectfully disagrees with the Examiner's assertions. The claims are clearly directed to an active matrix liquid crystal display device. As such, it is respectfully submitted that a new title need not be submitted."

While the title does describe the type of display to which the invention is directed, in light of the sheer volume of patents and patent applications directed to liquid crystal display devices, the title is not descriptive of the invention. There are currently over 100 US patents and US patent applications with titles containing the exact phrase "active matrix liquid crystal display device". There are another 100+ US patents and US patent applications with titles containing all the words in that phrase.

Regarding the claims, applicant argues:

"Bae and Greene, taken singly or in combination, fail to disclose or render obvious at least the claim features of "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row.., wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements." Bae is directed to forming a storage capacitor within a Liquid Crystal Display (LCD) without decreasing the aperture ratio of the display and without increasing the number of wires (see, e.g., Bae, column 2, lines 38-41). According to Bae, use of an independent storage electrode line (SL) within a row of pixels may decrease the aperture ratio of an LCD (see, e.g., Bae, column 2, lines 38-41) (see also FIG. 1, illustrating the use of an independent storage electrode line). Additionally, Bae describes prior art methods of circumventing the use of an independent storage line as being problematic because, in such methods, a connection between a terminal of a storage capacitor and a gate line generates a parasitic capacitance in the gate line (see, e.g., Bae, FIG. 2; column 2, lines 22,25). To avoid a decrease in aperture ratio and a parasitic capacitance, Bae proposes a liquid crystal display that has two or more storage capacitors (CsT) connected to drain terminals of switches (Q) of two different pixels of the display (see, e.g. Bae, column 2, lines 44-47; column 2, lines 60-64) (see also, e.g., Bae, FIG. 3). This configuration forms a line of storage capacitors along a row of pixels (see, e.g., Bae, FIG. 3). Bae recognizes that the configuration results in floating terminals of storage capacitors at the ends of the rows (see, e.g., Bae, column I 1, lines 37-40) and, to address the problem, Bae teaches a connection of the floating storage capacitor to a previous gate line (see,

e.g., Bae, column 11, lines 56'64) (FIGS. 23, 24).

However, Bae does not disclose "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row …wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements." Although Bae discloses a pixel configuration in which there is a connection between a floating storage capacitor and a gate line of a different row, the pixel configuration does not include a storage capacitor connected between a picture element electrode and a storage capacitor line. In the pixel configuration described in Bae, the pixel electrode (CLc terminal) (82) is directly connected to the line of storage capacitors (see, e.g., FIG. 23; column 8, lines 4-11 (describing the pixel electrode's relationship with the line of storage capacitors)). A storage capacitor is not situated between a picture element electrode and a storage capacitor line, as recited in claim 1."

However, for any given pixel, Bae teaches a storage capacitor connected between the picture element electrode and part of a storage capacitor line. The fact that the storage capacitor line is made up of the other storage capacitors is inconsequential. When one examines each pixel one at a time, every pixel can be defined as having a storage capacitor connected between the picture element electrode and part of a storage capacitor line.

The fact that Bae may teach away from a storage capacitor line as defined in the specification of the instant application, or that Bae may be solving a different problem is also inconsequential. The fact that applicant has recognized another advantage which

would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Furthermore, the claim does not require the storage capacitor line as defined in the specification nor claims the problem being solved as defined in the specification.

Applicant further argues:

"Indeed, the configuration of storage capacitors described in Bae cannot provide several beneficial LCD features that may, in contrast, be provided by aspects of the present principles. For example, according to aspects of the present principles, a storage capacitor line may be adapted to transmit both row address gating signals across a row of pixels and storage capacitor drive signals supplying a drive voltage across a row of pixels (see, e.g., Specification, p. 11, lines 17-26; p. 6, line 26 to p. 7, line 6) (see, also, FIG. 3, illustrating one configuration of a capacitor line 40 in accordance with one aspect of the present principles). This type of capacitive coupled drive scheme may improve the quality of the display by, for example, reducing image striking effects (see, e.g., Specification, p. 7, lines 2-6). Such signals cannot be transmitted through the line of capacitors disclosed in Bae, as the line itself is intermittently disjointed by storage capacitors (see, e.g., FIG. 24) (see also FIG. 9 & column 8, lines 7-11)."

However, the fact that Bae may be solving a different problem than the instant application is inconsequential. The fact that applicant has recognized another

advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., problem being solved as defined in the specification.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant further argues:

"Furthermore, it should be noted that modifying the configuration described by Bae to include a storage capacitor connected between the picture element electrode and a capacitor line is not obvious to one of ordinary skill in the art, as such a modification would subvert the entire principle of operation of Bae. As discussed above, Bae teaches the formation of a disjointed line of storage capacitors with terminals connected to different pixels to avoid a degradation of the aperture ratio of the display and a parasitic capacitance. Bae specifically teaches away from employing a storage capacitor between a pixel element electrode and a storage capacitor electrode line, as illustrated in FIG. 1 of Bae, because it states that use of the storage capacitor electrode line may

decrease the display device's aperture ratio (see, e.g., Bae, column 2, lines 9-12)."

However, no modification of Bae such as that proposed by the applicant is required. The claims do not claim the invention in such detail as to require Bae to be modified in the proposed manner.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the storage capacitor line consisting of a single continuous unbroken conductor extending from one side of the display to the other and not including any other electrical components such as capacitors.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, the fact that Bae may teach away from the invention does not change the fact that in teaching way, Bae still teaches the invention, and therefore can be used in a rejection.

Applicant further argues:

"Accordingly, Bae fails to disclose, suggest or render obvious the claim 1 feature of "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row...wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line

associated with a different row of picture elements."

In addition, Greene also fails to disclose or render these features of claim 1 obvious. Nowhere does Green disclose or remotely suggest use of capacitor lines shared by picture elements in the same row. Accordingly, Bae and Greene, taken singly or in any combination, fail to render claim 1 obvious."

However, as shown in the rejection and response to arguments above, Bae clearly teaches these limitations. Greene is merely being relied upon in the 103 rejection to teach the connection lines extending from one side of the array in the direction of the data address conductors. Furthermore, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further argues:

"According to Fujikawa, the described materials overlaying the signal lines avoid contact deficiencies resulting from oxidation of metal surfaces (see, e.g. Fujikawa, column 7, lines 50-52; column 7, line 65 to column 8, line 6; column 3, line 64 to column 4, line 11). Although Fujikawa mentions an LCD matrix having a storage capacitor connected between a capacitor line shared by pixel elements within a row (see, e.g., Fujikawa, FIG. 3), its combination with Bae by one of ordinary skill in the art would not result in "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row.., wherein the selection address

conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements," as included in claim 6."

However, as shown in the rejection and response to arguments above, Bae clearly teaches these limitations. Fujikawa is merely being relied upon in the 103 rejection to teach the capacitor line and selection address conductor for a particular row extending along opposite sides of the row of picture elements. Furthermore, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further argues:

"Firstly, the capacitor line configuration disclosed in Fujikawa is essentially the same as the configuration including an independent storage electrode line (SL) (Bae, FIG. 1) discussed in Bae. As stated above, use of such a configuration is specifically taught against by Bae because of its tendency to decrease a display device's aperture ratio."

However, the fact that Bae may teach away from the invention does not change the fact that in teaching way, Bae still teaches the invention, and therefore can be used in a rejection in combination with Fujikawa.

Furthermore, as stated above, Fujikawa is merely being relied upon to teach the location of the capacitor line. This location is being applied to the capacitor line comprising a plurality of capacitors connected in series as taught by Bae.

Applicant further argues:

"Secondly, even if the capacitor line configuration disclosed in Fujikawa was implemented, its combination with Bae by one of ordinary skill in the art would not result in the features of claim 6 recited above. As discussed above, the connection between a gate line of a previous row with the line of storage capacitors in the Bae LCD was made to address the problem of a "floating" storage capacitor at the ends of a line of capacitors in the proposed matrix configuration. If the capacitor line configuration disclosed in Fujikawa were implemented, the floating storage capacitor problem would be removed by virtue of the storage capacitor's connection between a pixel element electrode and the capacitor line.

As such, by combining Bae and Fujikawa, one of ordinary skill in the art would not conceive of "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row.., wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements," as included in claim 6."

However, as shown in the rejection and response to arguments above, Bae clearly teaches all these limitations of claim 6. As already stated above, Fujikawa is merely being relied upon in the 103 rejection to teach the location of the capacitor line. This location is being applied to the capacitor line comprising a plurality of capacitors connected in series as taught by Bae. Such a combination would have clearly been obvious to one of ordinary skill in the art at the time the invention was made.

Applicant further argues:

"In contrast to Bae, according to one aspect of the present principles, the coupling between a selection address conductor and a capacitor line associated with a different row may be made to avoid incongruent brightness levels resulting from parasitic capacitance associated with connection lines (see generally, Specification, p. 9, line 27 to p. 11, line 24). This exemplary feature is not disclosed or in any way even remotely suggested by any of the references."

However, applicant is reading the specification into the claims. The claims merely state the physical connections and locations of the connection lines connecting the capacitor lines and the selection address conductors. The claims do not claim a specific purpose or function of the connection lines.

Therefore, Bae teaches the connection lines, and Bae as modified by Greene teaches all of claims 1-5, and 7, and further combination with Fujikawa teaches all of claim 6.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. CARTER III whose telephone number is (571)270-3006. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/R.E.C./